



KINGS
COLLEGE OF ENGINEERING



DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

QUESTION BANK

SUB.NAME : VLSI DESIGN
BRANCH : EEE

SUBJECT CODE : EC 1354
YEAR/ SEMESTER : III / VI

UNIT – I

MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY

PART-A

1. What is meant by “Epitaxy”?
2. What is isolation?
3. What is the special feature of Twin-Tub process?
4. What are the various processes used in SOI?
5. What is silicide?
6. What is LDD?
7. What is LOCOS?
8. Give the advantages of IC?
9. What is Depletion mode Device?
10. Name the four generations of Integration Circuits?
11. Name the types of Integrated Circuits?
12. Give the basic process for IC fabrication.
13. What are the various steps in Silicon wafer preparation?
14. What are the advantages of Silicon-on-Insulator process?
15. What are the advantages of CMOS process?
16. What are the different MOS layers?
17. Why NMOS technology is preferred more than PMOS technology?
18. What are the different operating regions an MOS transistor?

PART-B

1. a) Explain the operation of NMOS Enhancement transistor? (8)
 b) Derive the Threshold voltage for NMOS Enhancement transistor? (8)
2. a) Explain about the body effect of MOS transistors. (6)
 b) Derive the design equations for MOS devices (4)
 c) What do you mean by channel length modulation (6)
3. a) Explain the second order effects with their equations. (10)
 b) Explain small signal AC characteristics with its design equations. (6)
4. Explain the fabrication of PMOS transistor and its substrate fabrication Process. (16)
5. Explain different fabrication process of CMOS transistor (16)

UNIT-II**INVERTERS AND LOGIC GATES****PART-A**

1. Define noise margin.
2. Define Rise Time.
3. What is body effect?
4. What is low noise margin?
5. What is stick diagram?
6. What are Lambda (O) - based design rules?
7. Define a super buffer.
8. Give the CMOS inverter DC transfer characteristics and operating regions
9. Give the various color coding used in stick diagram?
10. Define Delay time
11. Give the different symbols for transmission gate.
12. Compare between CMOS and bipolar technologies.
13. What are the static properties of complementary CMOS Gates?
14. Draw the circuit of a nMOS inverter
15. Draw the circuit of a CMOS inverter

PART-B

1. List out the layout design rule. Draw the physical layout for one basic gate and two universal gates. (16)
2. Explain the complimentary CMOS inverter DC characteristics. (16)
3. Write short notes on:
 - (a) Noise Margin (10)
 - (b) Rise Time (3)
 - (c) Fall Time (3)
4. Briefly discuss about the following:
 - a) Pseudo-NMOS inverter (8)
 - b) Saturated Load inverters (4)
 - c) Cascade inverter (4)
5. a. Explain the concept of static and dynamic CMOS design (8)
b. Explain the construction and operation of transmission gates (8)

UNIT III**CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION****PART-A**

1. What are the issues to be considered for circuit characterization and performance estimation?
2. Give the formula for resistance of a uniform slab of conducting material.
3. What are the factors to be considered for calculating total load capacitance on the output of a CMOS gate?
4. What are the components of Power dissipation?
5. What is meant by path electrical effort?
6. Define crosstalk.
7. Define scaling.
8. What are the factors to be considered for transistor scaling?
9. Define constant voltage scaling.
10. What are the sources to be considered for design margin?

PART-B

1. Explain in detail about the following:
 - a) Resistance estimation (8)
 - b) Inductance estimation (8)
2. Explain about routing capacitance with neat diagram. (16)
3. With neat diagram explain about power dissipation. (16)
4. Briefly explain about the following:
 - a) CMOS transistor sizing (8)
 - b) Design margining (8)
5. Explain about scaling of MOS transistor dimensions and charge sharing. (16)

UNIT –IV

**VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM
LEVEL PHYSICAL DESIGN**

PART-A

1. Write the difference between encoder and priority encoder.
2. Draw the CMOS implementation of 4-to-1 MUX using transmission gates.
3. Give the verilog coding for 4-bit magnitude comparator.
4. Draw the wheel floor plan
5. What is meant by clock distribution?
6. Design a circuit for finding the 9's compliment of a BCD number using 4-bit binary adder and some external logic gates
7. What is physical verification?
8. Mention the levels at which testing of a chip can be done
9. What are the approaches in design for testability?
10. What is known as boundary scan register?
11. Design a set of CMOS gates to implement the sum function.

PART-B

1. Give the design procedure for 8 bit carry look ahead adder. (16)
2. Design a multiplier for the given sequence: (16)

$$a_1 a_2 a_3 a_4 a_5 \times b_1 b_2 b_3$$

3. Draw the basic physical design for the inverter AND, OR and half-adder. (16)
4. Explain in detail about manufacturing of test principles. (16)
5. Explain the concept of clock distribution and power distribution. (16)

UNIT – V

VERILOG HARDWARE DESCRIPTION LANGUAGE

PART – A

1. What is Verilog?
2. What are identifiers?
3. What are gate primitives?
4. What is a FPGA?
5. Give the two blocks in behavioral modeling.
6. Define FSM.
7. Give the XILINX FPGA architecture
8. What is Switch-level modeling?
9. What is an antifuse?
10. What are the different types of modeling Verilog?

PART-B

1. Design a 4-bit carry look ahead adder and write the verilog HDL for it. (16)
2. Design 4X1 multiplexer and write the HDL for it in all four modeling: (16)
3. Briefly explain behavioral modeling(all functions) with an example: (16)
4. Design and develop a project in HDL to compare $x_5x_4x_3x_2x_1x_0$ with $y_5y_4y_3y_2y_1y_0$.
Check the output by means of test bench. (16)
5. Explain the following with an example:
 - i) Tasks and functions (4)
 - ii) Test bench for multiplexer (4)
 - iii) Difference between always and initial (4)
 - iv) Blocking and non-blocking statements (4)
6. Explain with a neat sketch the architecture of CLB'S available in xilinx XC 3000 series FPGA (16)
